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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
) Examiner: Not yet assigned
Jun-Fei Zheng et al.)
) Art Unit: Not yet assigned
Serial No.: Not yet assigned)
)
Filed: Herewith

For: WORK FUNCTION TUNING FOR MOSFET GATE ELECTRODES

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FORMAL DRAWINGS SUBMISSION

Enclosed herewith for submission in the United States Patent and Trademark Office are five (5) sheets of formal drawings for the patent application referenced above.

If there are any further charges please charge them to Deposit Account No. 02-2666. A duplicate of this sheet is enclosed for that purpose.

Respectfully submitted,

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Dated: 2/6, 2002

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Fig. 1

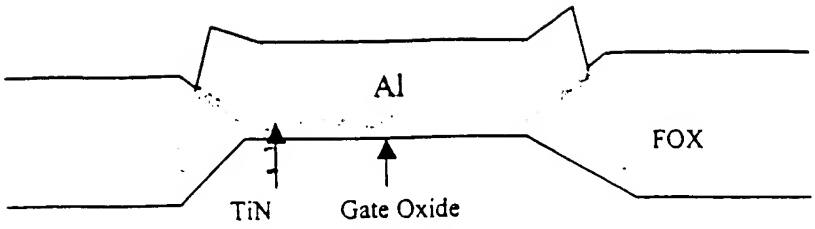


Fig. 2

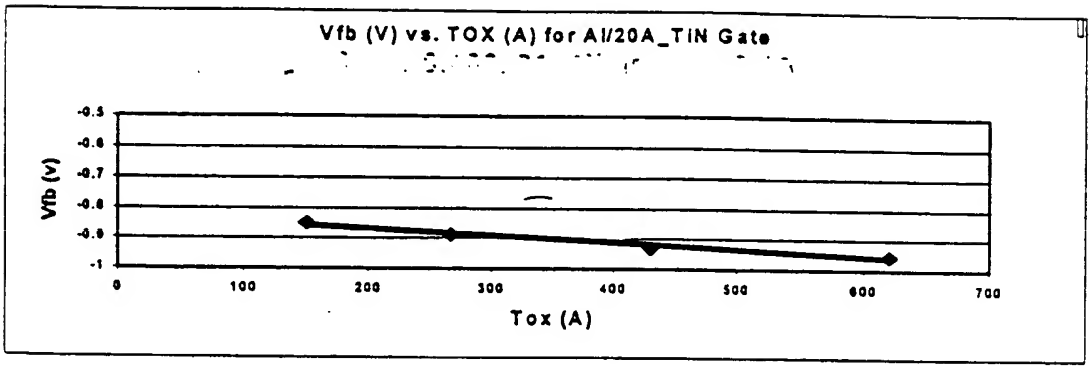


Fig. 3

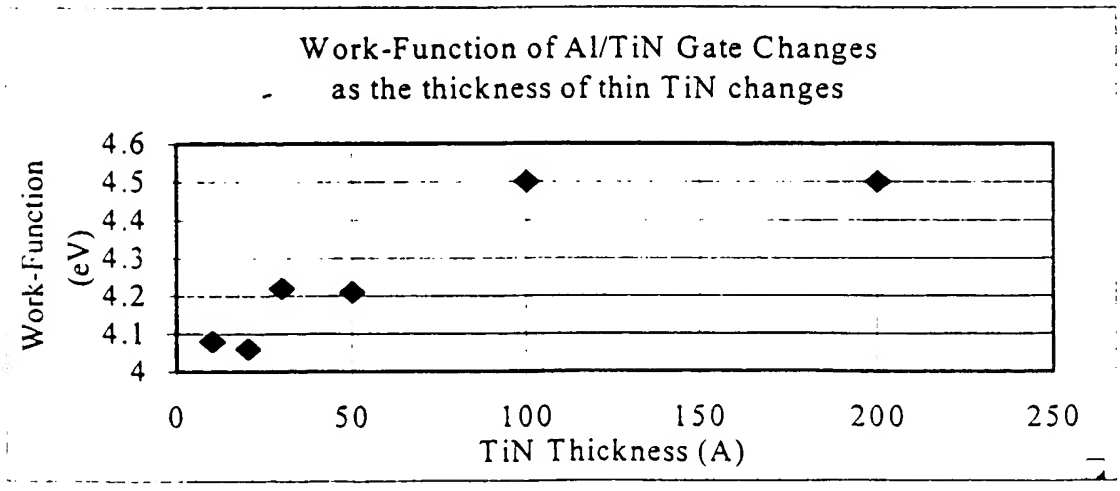
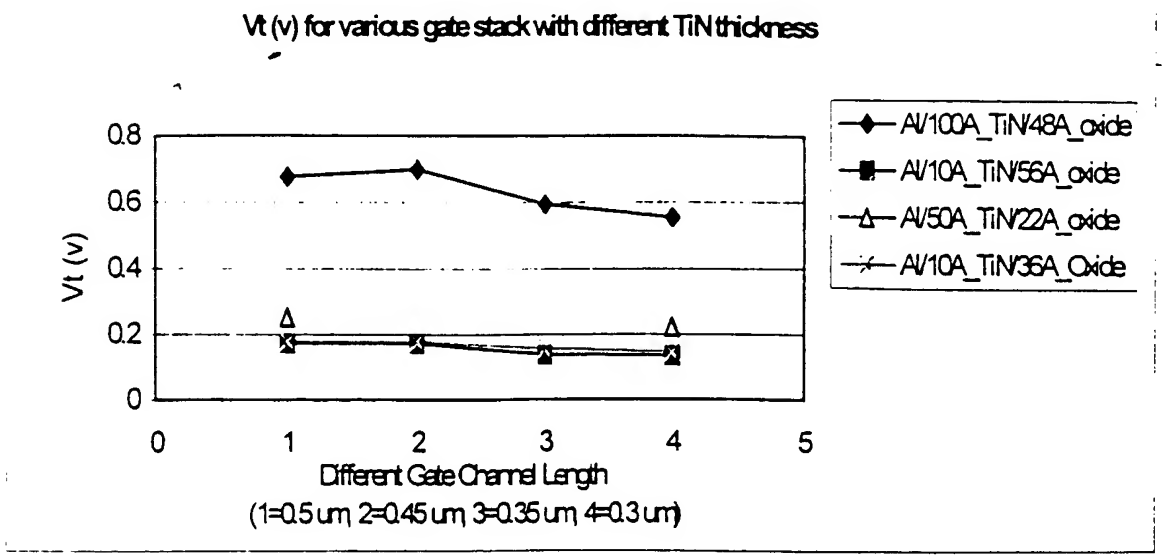


Fig. 4


Vt (v) for various gate stack with different TiN thickness
Vt (v)
0.8
0.6
0.4
0.2
0
0
1
2
3
4
5
Different Gate Channel Length
(1=0.5 um, 2=0.45 um, 3=0.35 um, 4=0.3 um)
Al/100A_TiN/48A_oxide
Al/10A_TiN/56A_oxide
Al/50A_TiN/22A_oxide
Al/10A_TiN/36A_Oxide

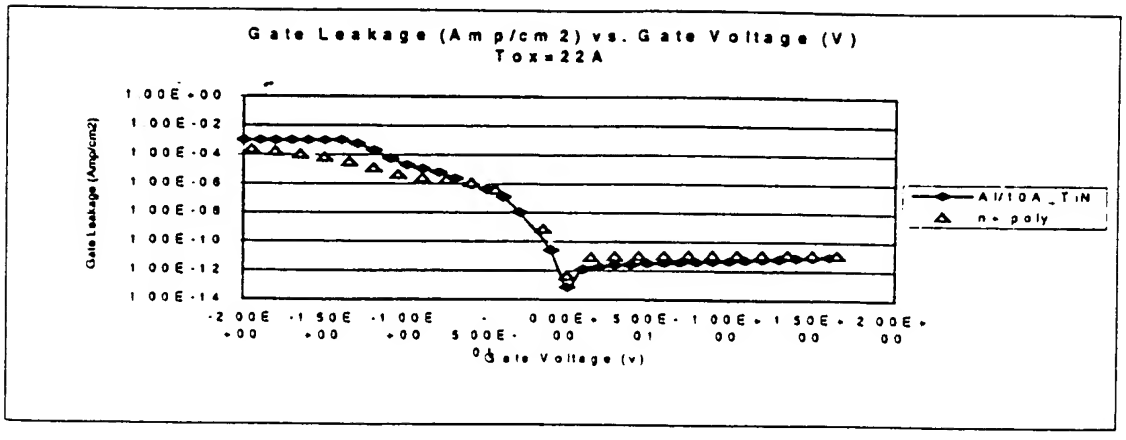

Gate Leakage (Amp/cm2) vs. Gate Voltage (V)
Tox=22A
Gate Leakage (Amp/cm2)
1.00E+00
1.00E-02
1.00E-04
1.00E-06
1.00E-08
1.00E-10
1.00E-12
1.00E-14
-2.00E+00
-1.50E+00
-1.00E+00
-5.00E-01
0.00E+00
5.00E-01
1.00E+00
1.50E+00
2.00E+00
Gate Voltage (v)
Al/10A_TiN
n+ poly

Fig.5

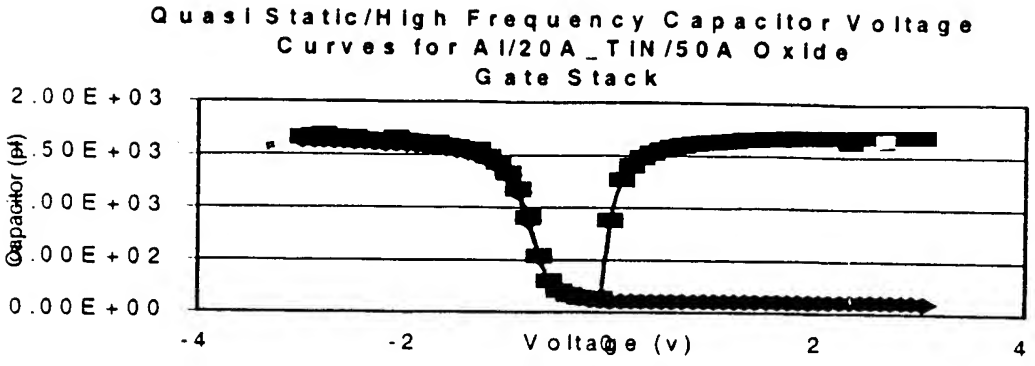

Quasi Static/High Frequency Capacitor Voltage Curves for Al/20A_TiN/50A Oxide Gate Stack
2.00E+03
1.50E+03
1.00E+03
5.00E+02
0.00E+00
Capacitor (pf)
-4
-2
0
2
4
Voltage (v)

Fig.6

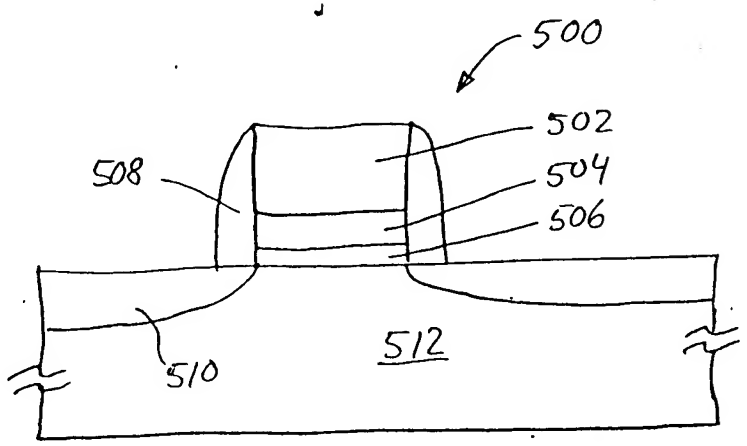


Fig. 7

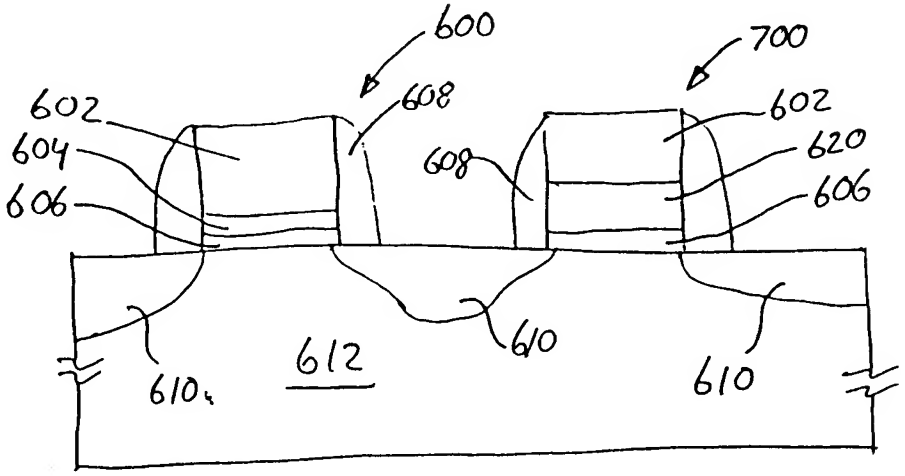


Fig. 8